APPLICATION NOTE

TDA8766G
EVALUATION BOARD DOCUMENTATION

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EVALUATION BOARD DOCUMENTATION

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Summary

This note describes a demonstration board which facilitates the evaluation of the TDA8766G 10 bit analog to digital converter (sections 2, 3, 4, 10, 11).
In addition the functionning of the TDA8766G is shortly described (sections 1, 5, 7, 8) and several methods to provide input offset and top and bottom references are shown (sections 5, 6).

CONTENTS

1. INTRODUCTION

The TDA8766G is a 10 bit high speed, low voltage, low power analog to digital converter (53 mW typical at 3.3 V, 4 mW in standby mode).
It has been designed for video signal digitizing, radio communication, camcorders & all applications where size and power saving are strong requirements.
The supplies can be set in the range of 2.7 V up to 5.25 V (down to 2.5 V for output supply). The sampling frequency can reach 20 MHz.
Digitizing of 10 Mhz full scale square wave signal (shape of CCD output signal) with the 10 bit resolution is allowed if the settling time (max. 6 ns) and the signal slope (max. 0.4 V/ns) are respected.
Application requires few external components.
TDA8766G comes in a plastic thin quad flat package LQFP32 (SOT401-1), with the following overall body dimensions: 5 x 5 x 1.4 mm^3.

The present demonstration board is intended to facilitate an evaluation of the main TDA8766 characteristics. It is realized with a three layer PCB (one internal ground plane).
The following features are included :

- 20 MHz on-board quartz oscillator or a connection for an external clock.

- ADC voltage supplies, analog input offset, top and bottom voltage references are adjustable by the means of potentiometers (PCB supply is 8 V).

- Connectors allow external voltage references & external output supply (VDDO).

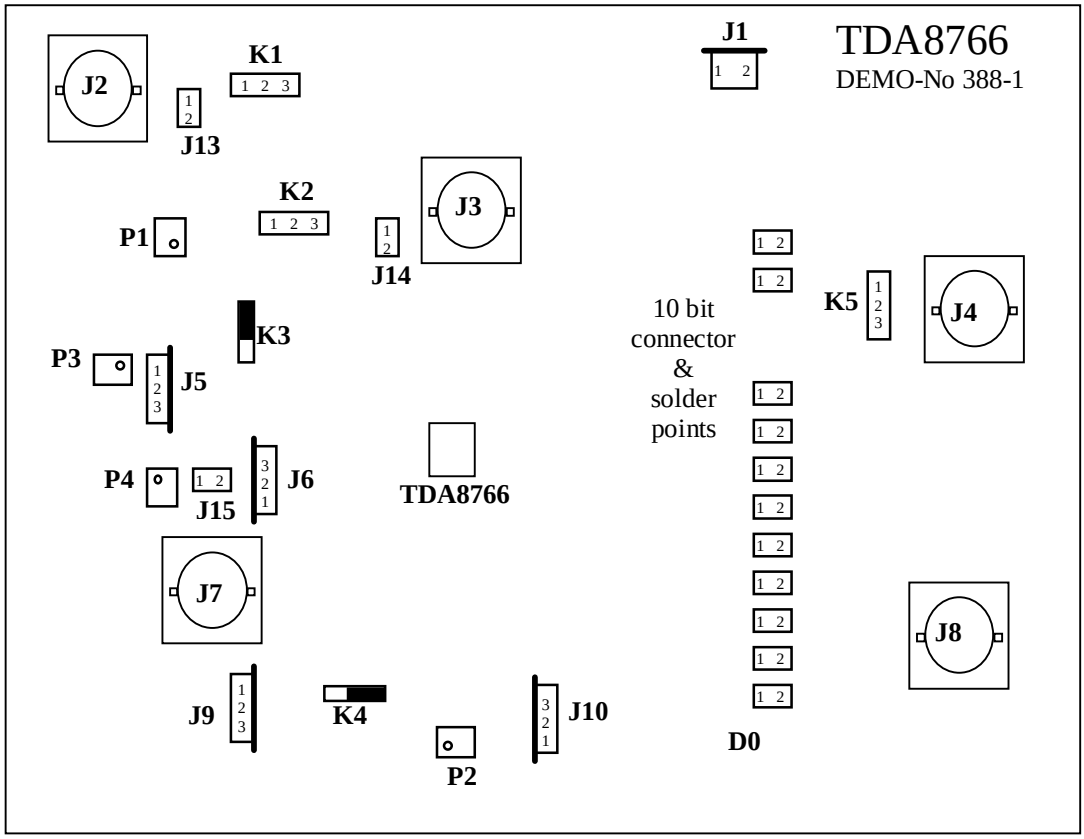
- DC or AC input signals are allowed. The input offset can be provided in three different ways :

  by a resistor bridge
  by a resistor connected to the middle reference voltage (pin 11)
  by an external voltage source

- A 10 bit D/A converter has been added on the board to verify the good operation of the ADC with an oscilloscope. Because this D/A converter is not perfect, its analog output should not be used to characterize the TDA8766G.

WARNING: the on board D/A converter does not withstand a low output load; so it is necessary to check the strobe/scope input impedance before connection.

2. CONNECTOR, SWITCH AND JUMPER POSITIONS



3. CONNECTOR SWITCH AND JUMPER LIST

Reference	Type	Function
J1	2 point connector	External board supply (8V)
J2	BNC	ADC (or ADC+DAC) clock input (50 Ω input)
J3	BNC	In range output (digital output)
J4	BNC	DAC clock input (50 Ω input)
J5	3 point connector/jumper	Internal/external bottom reference selection: J5.1,Ground J5.2,VBOT: Resistive load (1K potentiometer) must be connected with J5.3 if internal bottom voltage reference is used. J5.3,VBOT-ext: Pin for external bottom voltage reference connection.
J6	3 point connector/jumper	Internal offset (provided by VMED)/external input offset selection J6.1, IN-DC: This pin allows DC input connection or external input offset. J6.2, VMED: Vmedium voltage reference. Vmedium can be use to provide input offset (If it is well decoupled from the input signal by the R11, C1 cell). In that case J6.1 and J6.2 must be connected. J6.3, Ground.
J7	BNC	Signal input (50 Ω input)
J8	BNC	DAC output (high impedance probe is necessary)
J9	3 point connector/jumper	Internal/external top reference selection: J9.1, VTOP-ext: Pin for external top voltage reference connection, must be connected with J9.2 if internal top voltage reference is used. J9.2, Internal top voltage reference J9.3, Ground

Reference	Type	Function
J10	3 point connector/jumper	Internal/external VDDO supply selection J10.1,VDDO: Digital supply (VDDD), J10.2,VDDO-ext: External input for VDDO. TDA8766 accepts from 2.5V to 5.25V as the VDDO supply range. Must be connected with J10.1 if the internal VDDO is selected. If the internal VDDO is chosen, then VDDO=VDDD=VCCA. J10.3, Ground.
J13	2 point jumper	External clock **direct** connection Must be connected if external ADC clock is selected (In this case 5V to 3V logic level shifter is bypassed).
J14	2 point jumper	Clock test point
J15	2 point jumper	Internal input signal offset (provided by a resistor bridge) connection A resistor bridge (P4,R3,R7,C14) can be used to provide the input offset. In that case J15.1 and J15.2 must be connected. This resistor bridge is supplied by the top voltage reference.
K1 &K2	3 point jumpers	External/internal clock selection and 5V to 3V logic level shifter cell connection. K1.1 & K1.2 connection: J2 ADC CLK input is connected to the 5 to 3V level shifter cell and to the K5 jumper. K1.2 & K1.3 connection: Internal clock oscillator is connected to the 5 to 3V level shifter cell and to the K5 jumper. K2.1 & K2.2 connection: Direct connection between the external clock and the TDA8766 clock input is allowed. K2.2 & K1.3 connection: The 5 to 3 V logic level shifter cell output is connected to the TDA8766 clock input.

Reference	Type	Function
K3	switch	Stand-by control Upper position STB=0 (standby off) Lower position STB=1 (standby on)
K4	switch	Output enable Left position OE=1 (output high impedance) Right position OE=0 (chip enabled)
K5	3 point jumper	Internal/external clock selection for the DAC K5.1 & K5.2 connection: Internal or ADC clock selection K5.2 & K5.3 connection: External DAC clock (J4) selection.

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4. INITIAL SETTINGS : 3.3 V ADC SUPPLIES, AC COUPLED INPUT, 20 MHz CLOCK (ON BOARD), 3.3 V and 1.2 V VOLTAGE REFERENCES

The board supply must be set at 8 V.

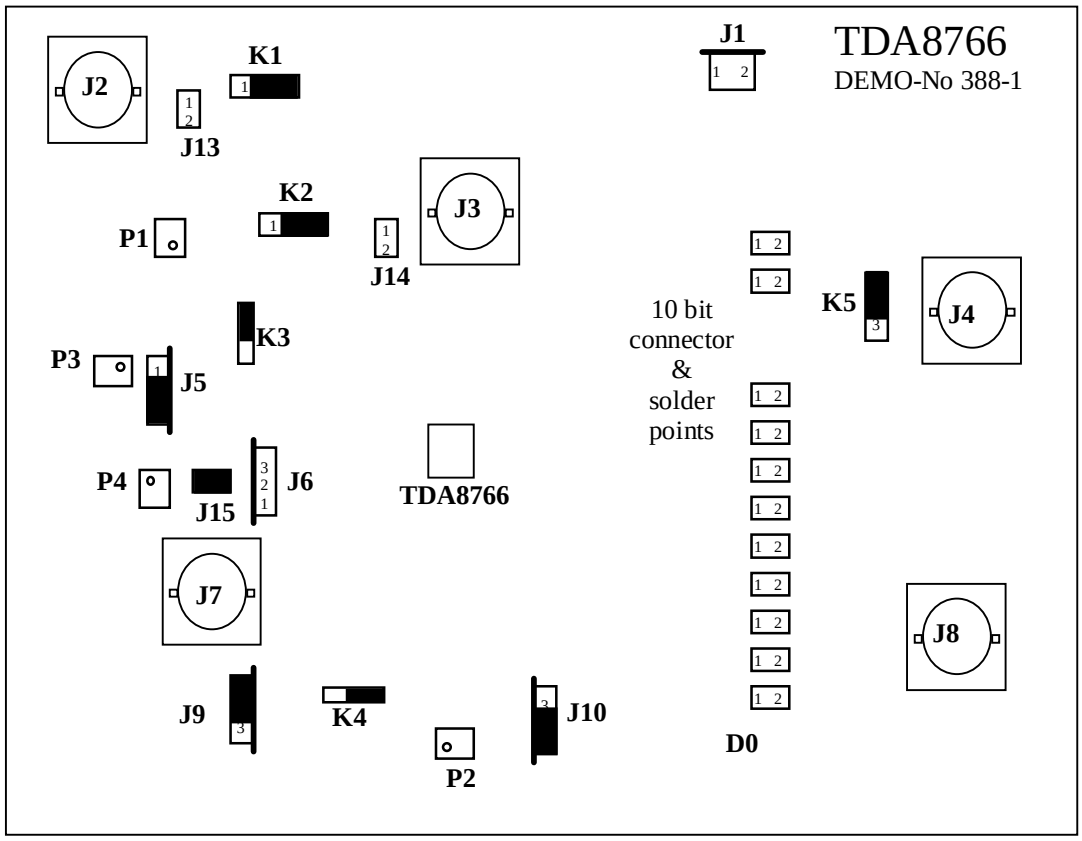
In this configuration the analog input signal source must be provided by an external generator which is connected to the board by the J7 connector (dynamic input impedance: 50 Ω).
The ADC supplies are provided by an adjustable precision regulator (TL431, IC6).
The ADC supplies are adjustable from 2.7 V (2.5 V for VDDO) up to 5.25 V by the means of the P2 potentiometer.

The analog signal input offset is derived from the ADC analog supply through a resistor bridge (R7,R3,C14, and potentiometer P4). It is adjustable thanks to P4.
Top & bottom voltage references are provided simply and economically :

The top reference voltage is provided by an adjustable precision regulator (TL431, IC3).

The bottom reference is provided by a simple resistor load (potentiometer P3). The top and bottom reference can be adjusted by the means of P1 and P3 potentiometers respectively.

To obtain this operational mode, jumpers and switches are set as shown in the following figure.



Potentiometers P1, P2, P3, P4 are adjusted as explained in the following.

P1 is used for the top reference voltage adjustement. To obtain 3.3V, P1 is set around 157 Ω.

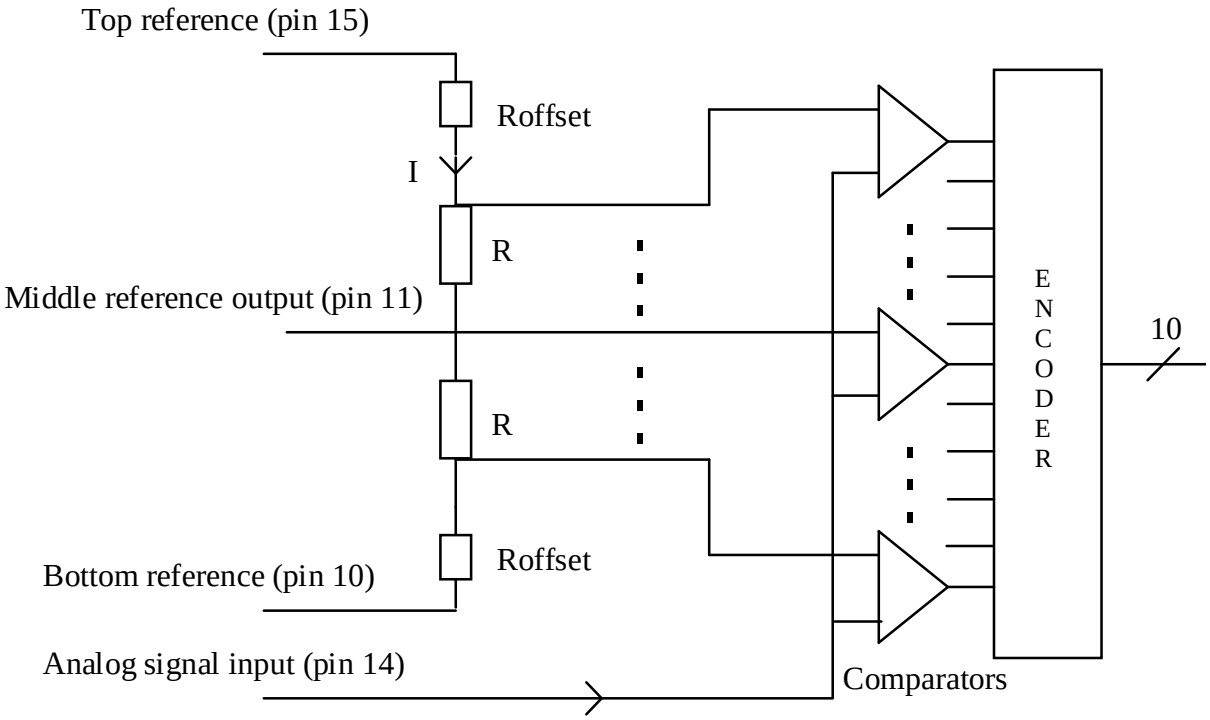
P2 potentiometer is used to adjust the ADC and the 74LVC86D supplies. In order to obtain 3.3 V supplies, P2 is adjusted around 157 Ω. (See section 8 for more information about supplies)

P3 allows the adjustment of the bottom voltage reference. In order to obtain a bottom reference of 1.2 V, P3 is adjusted around 165 Ω. See section 5 for more information about references.

P4 allows the adjustment of the input offset. In order to obtain an input offset of 2.25 V, P4 is adjusted around 2093 Ω. (See section 6 for more information about input offset)

5. VOLTAGE REFERENCES

Here is a block diagram which explains the TDA8766 working:



During the A to D conversion the analog input signal (pin14) is compared to voltage references by the means of voltage comparators (In fact these comparators are folding amplifiers).

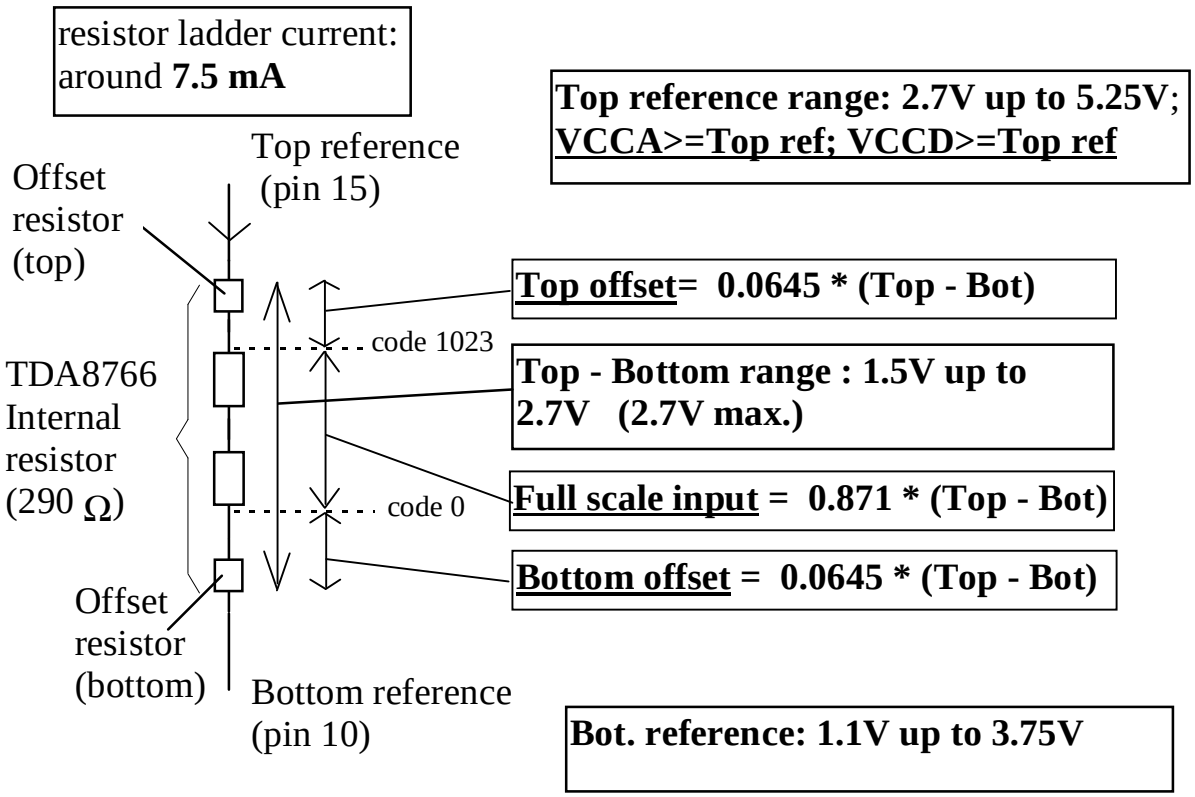
The full scale analog signal input range (FS) is given by:
FS=0.871 (Top ref. - Bottom ref.) ; The 0.871 coefficient is due to the two offset resistors.

The comparator voltage references are derived from a resistor ladder which is supplied through Vtop (pin 15) and Vbottom (pin 10). Therefore if the Vtop and Vbottom are not well regulated the A to D conversion will be affected.

Top reference (pin 15) is the highest voltage reference and the bottom reference (pin 10) is the lowest voltage reference. Consequently a current I is flowing from pin 15 to pin 10.

The typical value for the internal resistor ladder is 290 Ω at 25°C.

As shown in the following schematic the TDA8766 is versatile in the choice of the top voltage reference, bottom voltage reference and power supplies. So it will be easy to find top and bottom voltage references which fit with the majority of the applications.

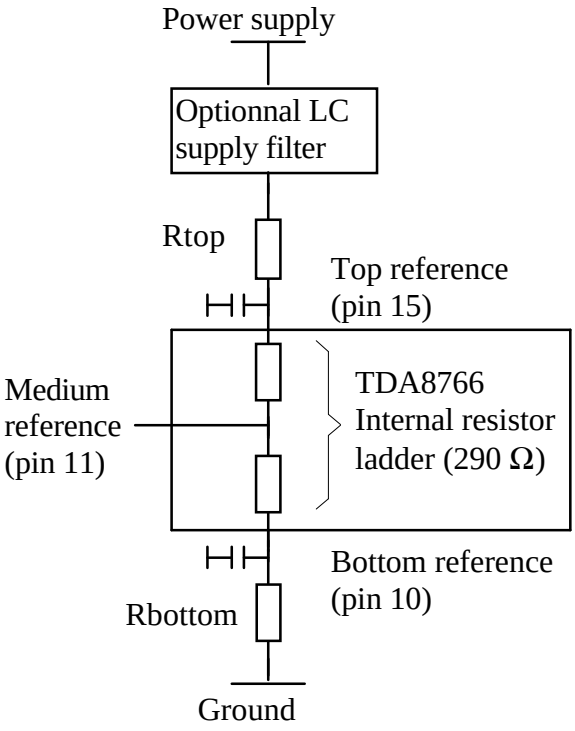


Regulation of Vtop & Vbottom depends on the level of cost and quality that are required by the customer application.

Several methods providing these voltage references are shown in this section.

5.1 TOP AND BOTTOM REFERENCES DERIVED FROM A POWER SUPPLY

If the power supply is well regulated a simple resistor string stucture will be efficient (see following figure).



It is possible that the top reference equal the power supply voltage. So the Rtop resistor can be removed. An optional filter can be added on the analog supply (depending on supply noise level).

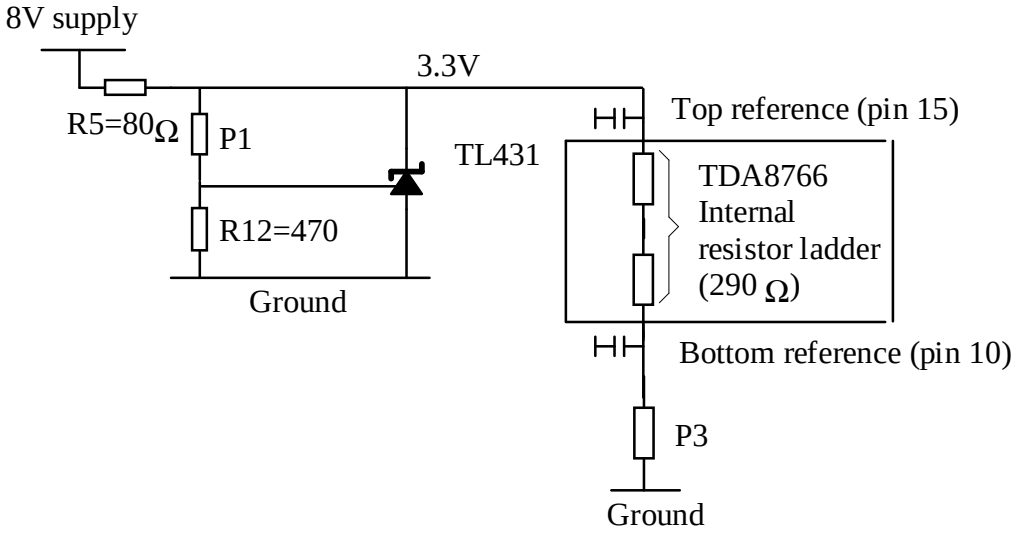
Typical voltages for a 3.3V application are 3.3V for the top reference and 1.2V for the bottom reference
The current flowing through the 290 Ω resistor ladder is 7.24 mA. So Rtop=0 and Rbottom=160Ω.

Remarks: here, the spreads due to process and temperature are not taken into account.

5.2 TOP AND BOTTOM REFERENCES DERIVED FROM REFERENCE VOLTAGE REGULATOR(S)

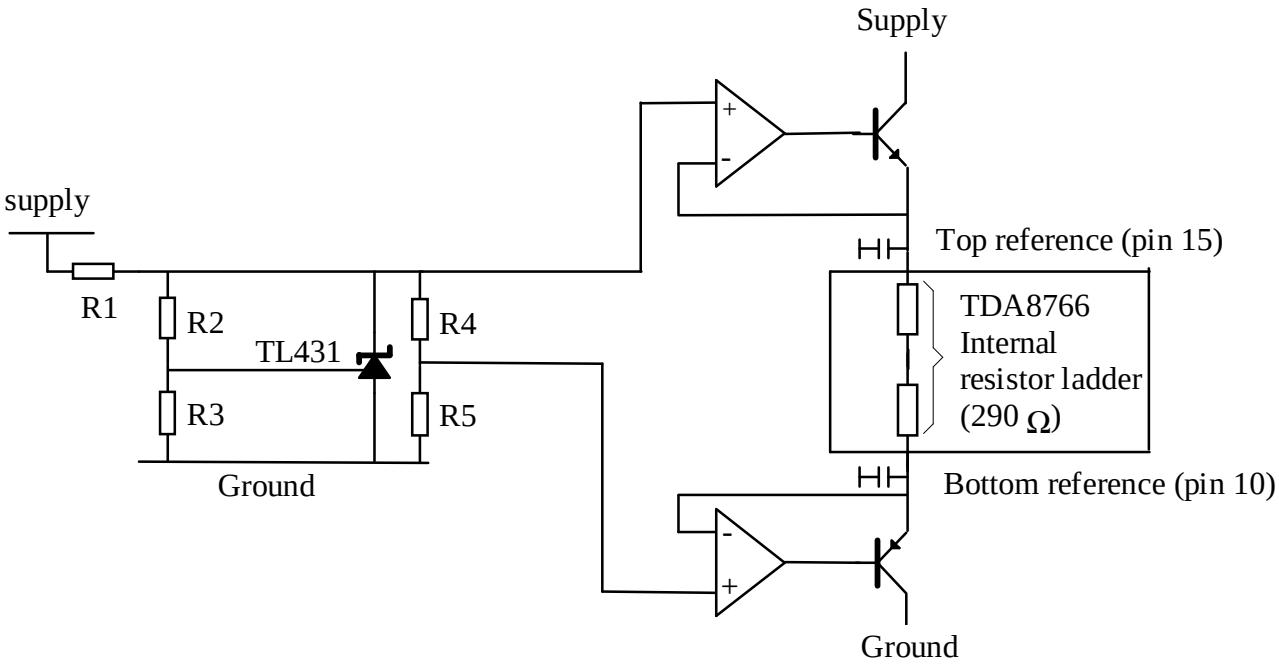
In some cases (noise on supply, several ADC's mounted in parallel ...) solutions with precision regulators (Philips uA723, Texas TL431,...) may be preferred.
On this board a regulator for the top voltage reference is provided (IC3,TL431), whereas the bottom reference is simply provided by a potentiometer (P3):

TL431 output=2.5 *(1+P1/R12) V



Two connectors on the board, J9 (for top reference) and J5 (for bottom reference), allow connection of external references.

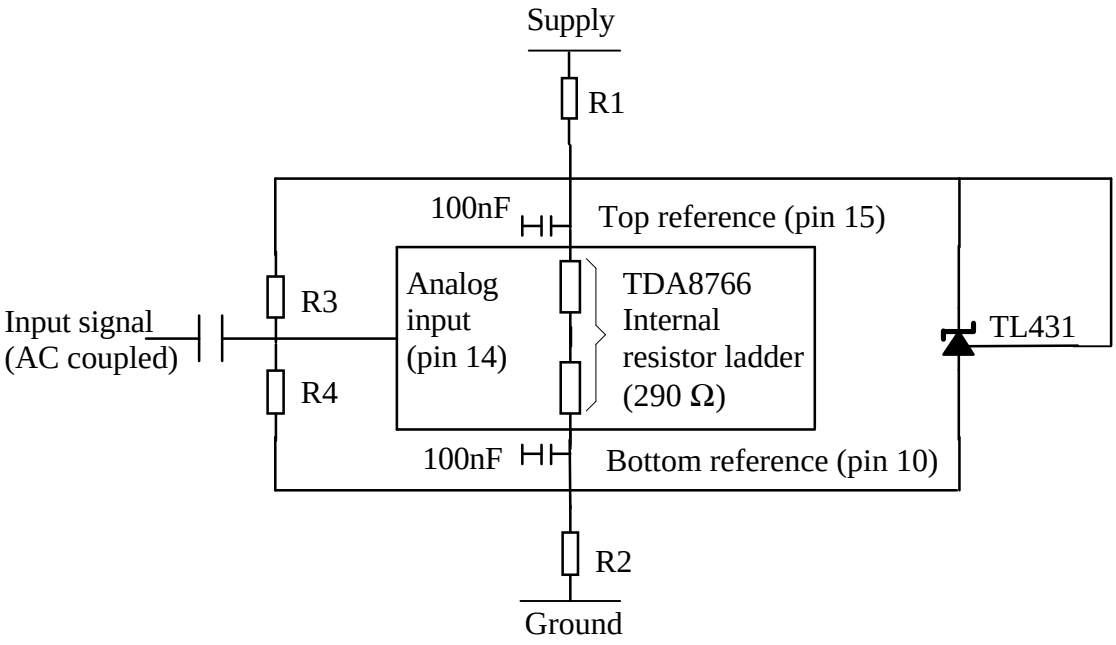
If several ADC are mounted in parallel, or if a very high precision of the voltage references over the whole temperature range is required, the following schematic can be used :



Operational amplifier with a low input offset should be used. The transistor types depend on the number of TDA8766G mounted in parallel. (7.5 mA typ. for one TDA8766G)

If only one ADC is used the operational amplifier and the transistor which drives the top reference can be skipped. In this case, the voltage regulator directly drives the top reference.

In the following electrical diagram, top and bottom references are regulated by only one component (TL431):



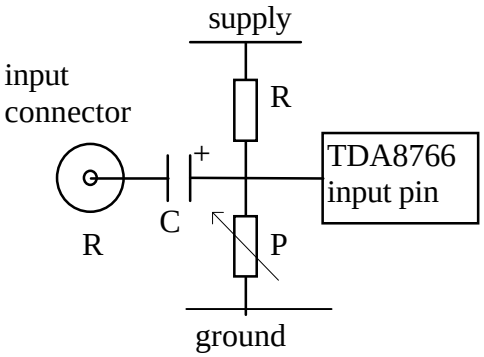
The (top - bottom) difference is set at 2.5V by the TL431, so the full scale input is set at 0.871*2.5=2.18V. In addition the input offset is set at (Vtop+Vbottom)/2 by two equal resistors (R3 and R4).
In this case the TL431 maintains the (top - bottom) difference at 2.5V over temperature and supply variations. Because the input offset is derived from the top and bottom references, it is also regulated at (Vtop+Vbottom)/2 over the temperatureand supply variations.
Using this method it is possible to drive the input offset and the top and bottom references of several TDA8766G with a very good matching with only one TL431.
Typical resistor values for a 5V application and for one TDA8766G are:
R3=R4=2.2KΩ, R1=R2=82Ω. The current flowing trough the R1, R2 resistors is around 15mA (The TL431 requires a minimum current to provide a good regulation).

6. INPUT OFFSET

When AC coupling is used with the TDA8766 it is necessary to provide an input offset in order to respect the TDA8766 full scale input range.
Relations between the Vtop reference,the Vbottom reference, the maximum amplitude of the analog signal and the input offset are:
Maximum amplitude of analog signal is (Vtop-Vbot)* 0.871 and the input signal is centered around the input offset which is (Vtop+Vbottom)/2.
Consequently, if Vtop = 3.3 V and if Vbottom = 1.2 V the maximum amplitude of the analog signal is 1.83 V and the input offset is 2.25V; code 0 is obtained for a 1.335V input, and code 1023 is obtained for a 3.165 V input.

Input offset can be provided by many different methods; several methods are explained in this section.

6.1 INPUT OFFSET DERIVED FROM A RESISTOR BRIDGE



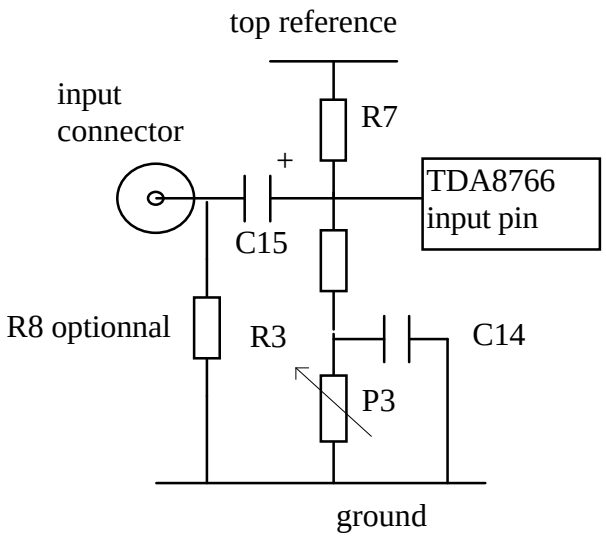
When a resistor bridge is used to provide an offset the current flowing through the resistors must be at least 10 times greater than the signal current (TDA8766 analog input current is 0 to 35 µA) in order to guarantee the stability of the input offset. Consequently the resistive value of this resistor string must be below 8.5 kΩ (with a 3 V supply).

If the input signal generator used to test the TDA8766 requires a 50 Ω load, R must be set at 73.33 Ω and P at 157.14 Ω (Vtop=supplies=3.3 V,Vbottom=1.2 V), in order that the dynamic impedance (R & P in parallel) be 50 Ω.

Remarks:

- This method provides a correct input offset but the current flowing through the resistor bridge is high: 14mA (R=75Ω, P=157Ω and 3.3V supply).

In order to reduce this current consumption another method is used on board but it requires two more components (one capacitor and one resistor) :



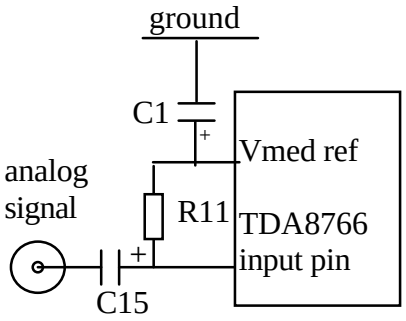
R3 is equal to the output load of the external signal generator. C14 allows ground connection between R3 and P3 in dynamic mode. Typical values when a 50 Ω signal generator is used are: R7=1K Ω, R3=50 Ω, P3=5 kΩ (set at 2093 Ω), C14=10 nF, then the current flowing through the resistor bridge is only 1.05 mA with a 3.3 V top reference.
The solder print of an optional resistor R8 is provided in order to allow other impedance adaptations.

- When it is possible, it is better to replace the potentiometers by fixed resistors. This will avoid possible distortion effects on the input signal due to the capacitive components of the potentiometers.

- It can be difficult to obtain the exact output load and the exact input offset when they are made up of fixed resistors, because the accuracy of the resistors is limited. Consequently in some professional applications it is better to provide the correct load and the correct input offset by means of operational amplifiers.

6.2 INPUT OFFSET DERIVED FROM THE MEDIUM REFERENCE

In this case the input pin is connected to the medium voltage reference (pin 7) by the means of a resistor (R11). The medium voltage reference must be well decoupled by a capacitor (C1). The input impedance of the AD converter is given by R11 in parallel with Zin.



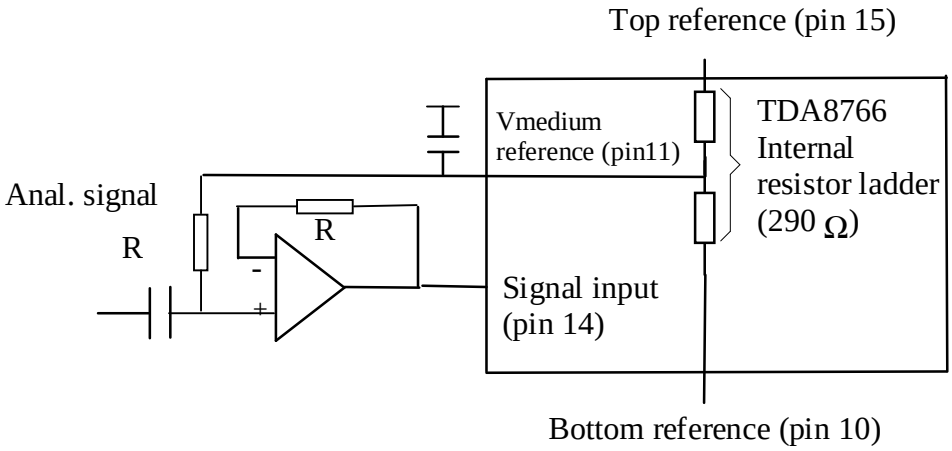
This method gives good results in the following domains : high common mode supply rejection (because both the voltage references and the input offset are derived from the same supply), very low noise level and low cost.
R11*C1 product must be high enough in order to avoid a coupling between the input signal and the medium reference.
(C1=4.7µF for example)
The offset on the input pin is:
Vmed - (17µA*R11)

On board selection of the input offset, provided by the medium reference, is allowed by the J6.1 & J6.2 connection. In this case R11 and C1 must be soldered (SMD 1206 series solder prints).

6.3 INPUT OFFSET PROVIDED BY AN OPERATIONAL AMPLIFIER

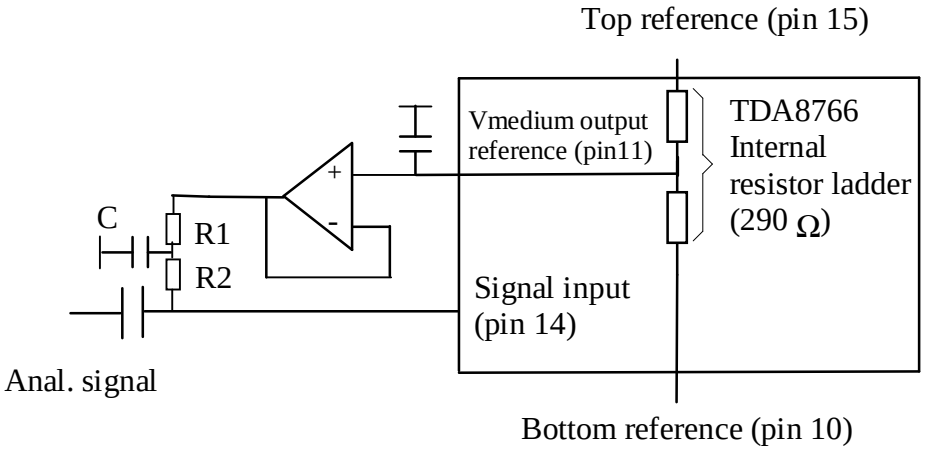
The middle output reference voltage and a low input offset operational amplifier can be used to provide an accurate input offset. Several methods can be used :

1°)



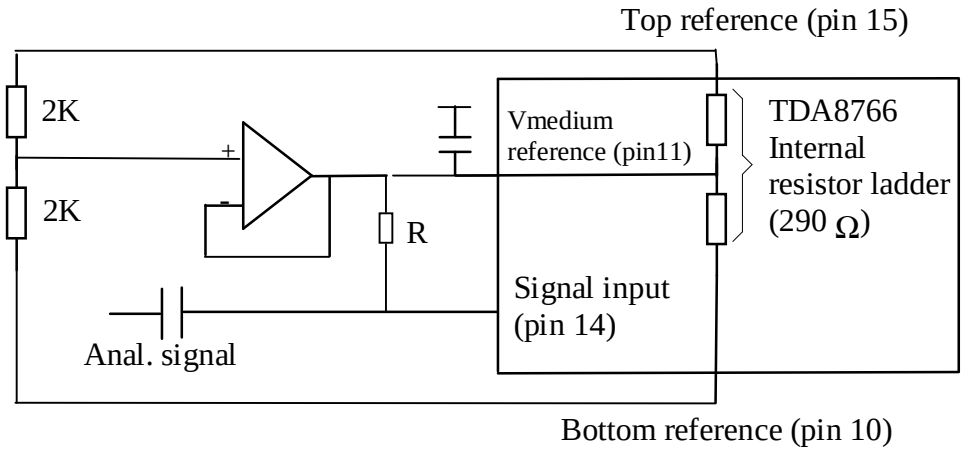
The R resistor in the op-amp loop compensates the offset due to the R resistor connected to Vmed. (R=1kΩ; C=1µF)

2°)



The amplifier does not need a high bandwidth, but the necessary time to load the C capacitor at ‘power on’ depends on.the op.amp maximum output current. The input impedance is R2 // Zin. Zin is the ADC input impedance.

3°)

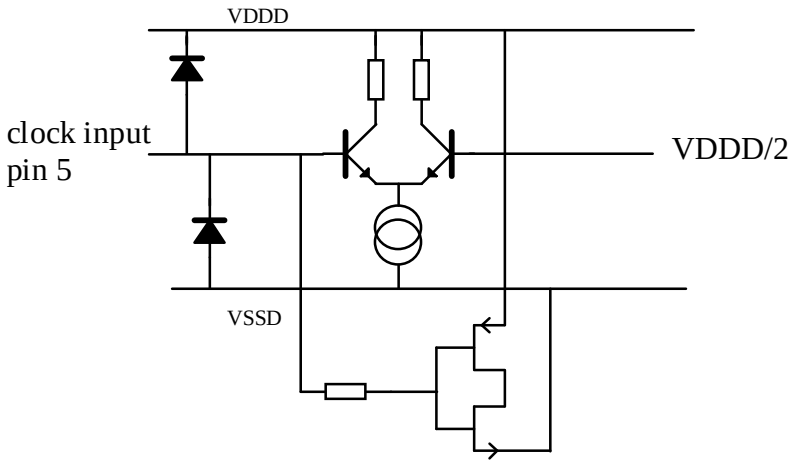


Medium reference is derived from top and bottom reference (input impedance is R // Zin).

7. CLOCK

7.1 CLOCK INPUT

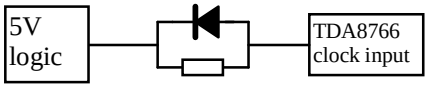
On the demo-board several methods can be used (depending on switch positions) to provide the ADC clock (see sections 2,3). Precautions must be taken if the high clock level is higher than the VDDD level.
In fact, the TDA8766 clock input (pin 5) is protected by diodes (see figure):



If the high clock level is greater than VDDD+0.5 V, a current will flow between the clock input & VDDD through the protection diode. This will affect the proper functioning of the ADC.
Consequently, it is necessary to keep the high clock level below VDDD+0.5 V.
Several methods can be used to limit high clock level :

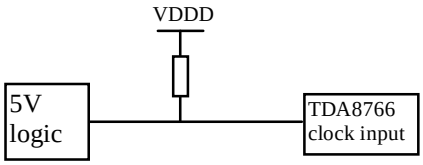
1- Use of a 3 V logic device as a 5 to 3 V interface (Philips LVC logic family for example).

2- Use of a parallel resistor/diode network in series with 5 V output.



The resistor limits current and voltage supplied to the TDA8766. The diode allows a faster high to low transition (R=470Ω, D=BAS16/BAS32...).

3- In case of 5 V logic with an open drain output, use a pull-up resistor connected to the low voltage supply.



For each method It is possible to test the influences on ADC performance of each method with the demo-board. A 74LVC86D is used as a 5V logic to 3V logic level translator. SMD resistors and diodes solder prints are provided to allow the testing of the diode/resistor network (R2, D2) and the testing of the pull-up resistor (R1).

ON BOARD / EXTERNAL CLOCKS SELECTION (SUMMARY):

IC2 (low voltage logic xor gates), K1, K2, K5,J13 (jumpers), R1, R2, R4, R6 (resistors), D2 (diode), allow a wide choice of ADC & DAC clock sources.
The following settings are possible :

- A 20 MHz TTL on-board quartz oscillator can be chosen with K1 & K5.

- Direct external clock connection is also possible by means of the J2 & J13.

- On board or external clock can be used independently for both ADC & DAC.

- The clock can be connected directly to the ADC or through a 5V to 3V logic interface (R2, R1, D2, IC2).Therefore, logic with open collector output, standard CMOS logic, or standard TTL logic, can be connected to the board.

7.2 CLOCK JITTER

If the clock jitter and the slope of the analog input signal are high, sampling errors can appear.

Example :

The equation of a sinewave signal is **$s(t)=A/2 \sin(2 \pi F t)$**, where **A** is the ADC full scale amplitude (**A=1024 LSB**) and **F** is the sinewave frequency.
The slope of this signal is given by: **$ds(t)/dt=A/2\ 2 \pi\ F \cos(2 \pi F t)$**
This slope is maximum when t=0 (input voltage level is around middle code 511/512):
$ds(0)/dt=A \pi\ F$ Volt/second.
That means that the middle code is available at the ADC input only during:
$Tlsb=LSB/(A \pi F)=(1024 \pi F)^{-1}$ second.
If the full scale sinewave frequency is **F = 10 MHz**, then **Tlsb = 31 ps**
Consequently the clock jitter must be lower than this value.
If a 20 Mhz full scale sinewave is sampling the jitter must be lower than 15 ps.

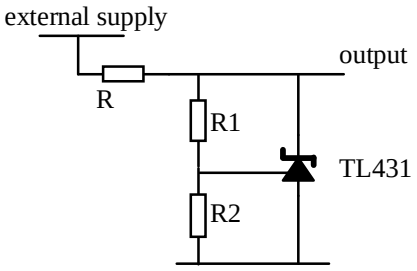
Remarks:

If the sample clock frequency and the input signal frequency have the same jitter (or phase noise), the sampling error due to jitter can be avoided. Therefore it is not suitable to do precise dynamic measurements of the ADC characteristics with the on board quartz oscillator. (Except if the input signal frequency and the quartz oscillator frequency are correlated).

8. ADC SUPPLIES

ADC and 74LVC86D supplies are provided by an adjustable voltage regulator (TL431,IC6).

The DAC supplies are set to 5 V (by the means of a 7805 regulator).
The IC6 regulator output voltages are adjustable by a resistor ratio (see figure).
The formula which gives the regulated voltage related to the resistor ratio is :



Vout=2.5*(1+R1/R2)

The power consumption of each TL431 is volontarily set higher than necessary in order to allow different ADC voltage supplies. See section 10: how to change the ADC supplies.

9. 10 BIT D/A CONVERTER

A 10 bit 5 V supply/TTL input DAC (IC5) allows **rough** ADC evaluation with a scope or a spectrum analyzer. Analog output level is in the range of 3 to 5 V.

WARNING: This D/A converter does not support low output loads, so it is necessary to check the strobe/scope input impedance before connection to the load.

10. HOW TO CHANGE THE ADC SUPPLIES

The TDA8766G can work with all supply voltages in the range of 2.7 V to 5.25 V: analog supply (VDDA), digital supply (VDDD), output supply (VDDO). Furthermore, VDDO can be set as low as 2.5 V.
The only restriction for the supplies is to respect the following conditions:

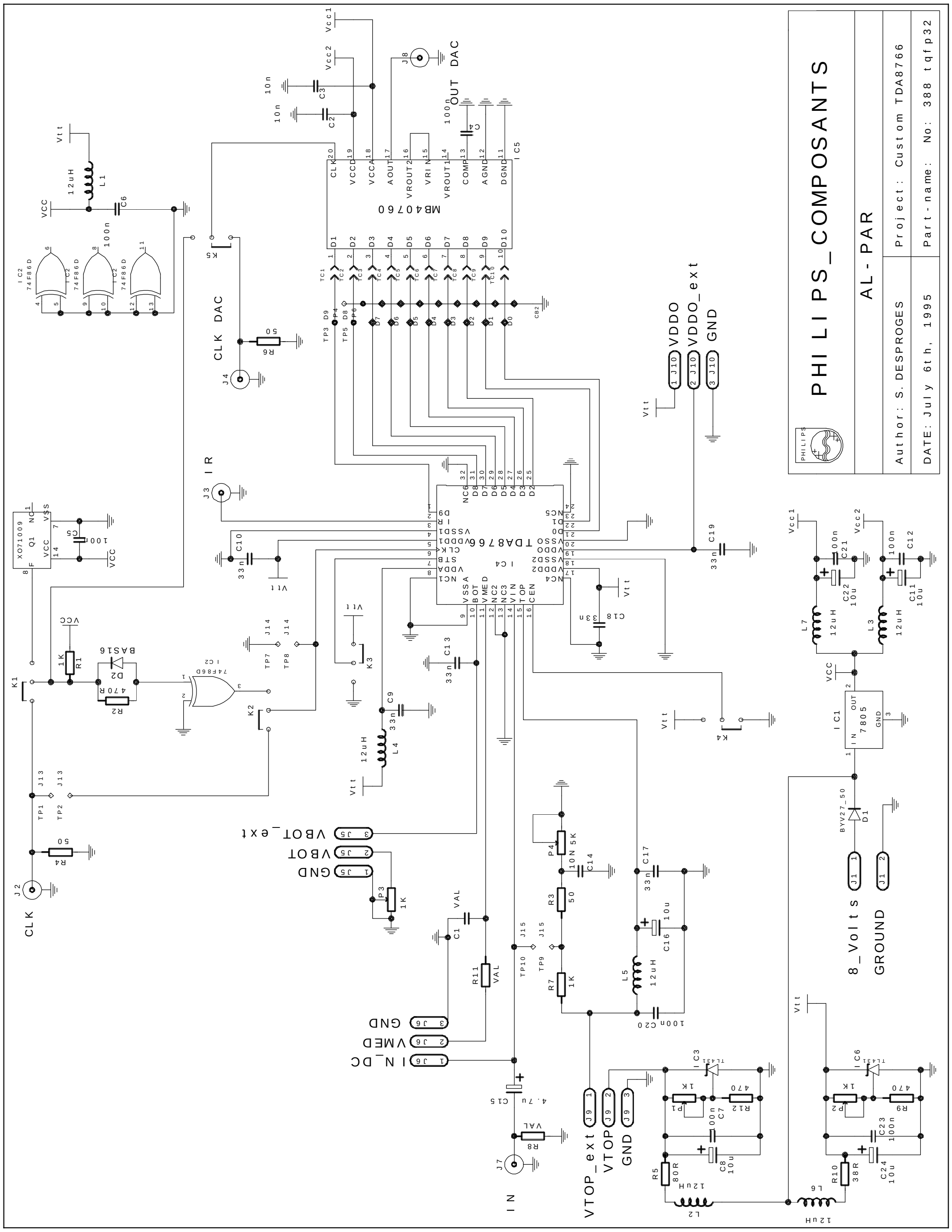
-0.2V < VDDA-VDDD < 0.2V
-0.2V < VDDD-VDDO < 3V
-0.2V < VDDA-VDDO < 3V

Adjustment of the ADC supplies in the range of 2.7 V to 5 V is achieved by the adjustment of P4 potentiometers (see section 8).
Separate adjustment of VDDO is possible if an external supply is connected to J10. Be sure to respect the limit differences between the supplies.

11. DEMO BOARD DOCUMENTATION : ELECTRICAL DIAGRAM, COMPONENT LIST & COMPONENT PLACE

11.1 ELECTRICAL DIAGRAM

(see next page)


PHILIPS_COMPOSANTS
AL-PAR
Author: S. DESPROGES
DATE: July 6th, 1995
Project: Custom TDA8766
Part-name: No: 388 tqfp32

11.2 COMPONENT LIST

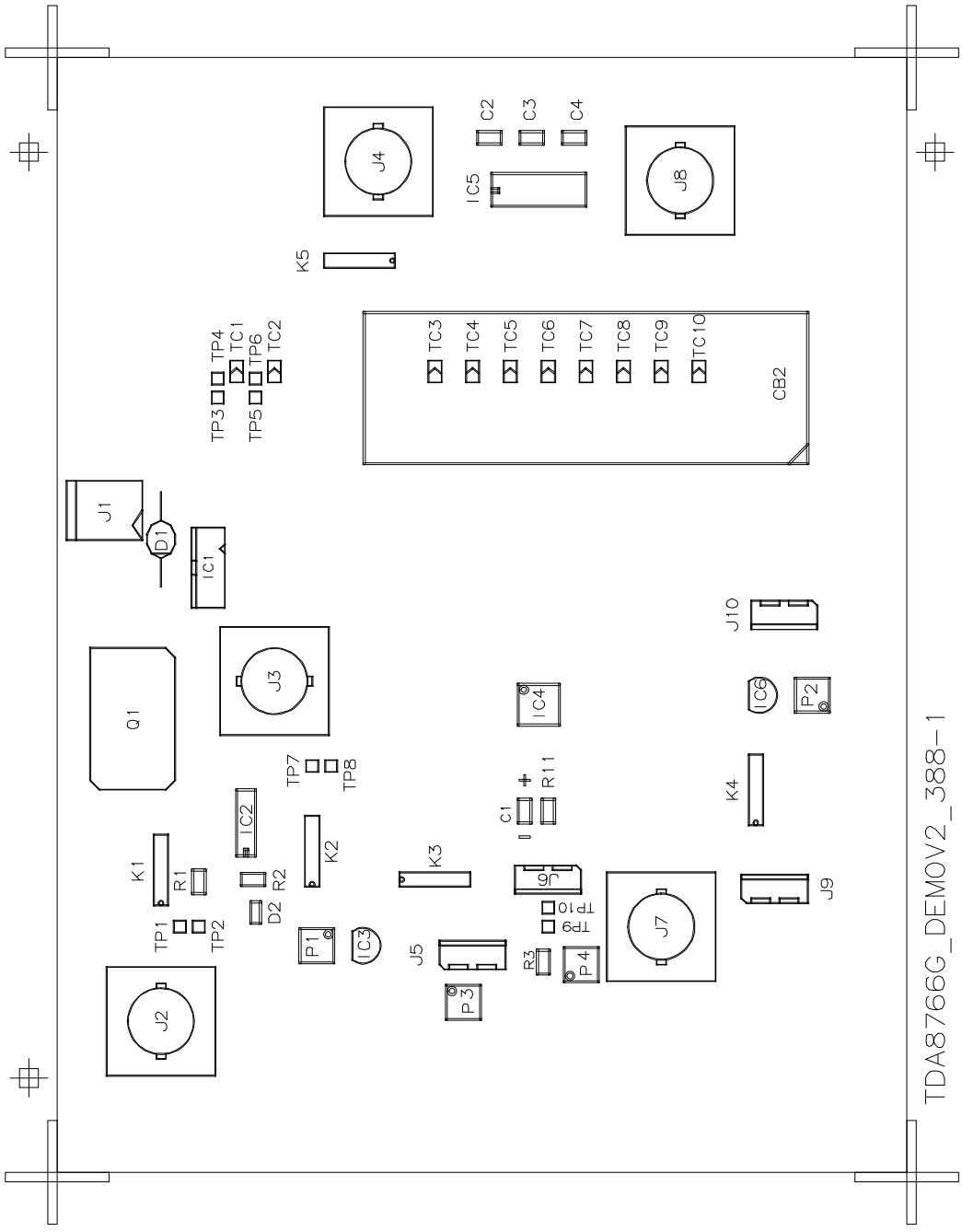
Reference	Value	Component
C1	1 µF	SPRAGUE_595D_A
C2	10 nF	C1206
C3	10 nF	C1206
C4	100 nF	C1206
C5	100 nF	C1206
C6	100 nF	C1206
C7	100 nF	C1206
C8	10 µF	SPRAGUE_595D_A
C9	33 µF	C805
C10	33 nF	C805
C11	10 µF	SPRAGUE_595D_A
C12	100 nF	C1206
C13	33 nF	C805
C14	10 nF	C805
C15	4.7 µF	SPRAGUE_595D_A
C16	10 µF	SPRAGUE_595D_A
C17	33 nF	C805
C18	33 nF	C805
C19	33 nF	C805
C20	100 nF	C1206
C21	100 nF	C1206
C22	10 µF	SPRAGUE_595D_A
C23	100 nF	C1206
C24	10 µF	SPRAGUE_595D_A
CB2		8 BITS CONNECTOR (LSBs)
D1		BYV27_50
D2		BAS16/BAS32
IC1		T7805CT
IC2		74LVC86D
IC3		TL431
IC4		TDA8766
IC5		MB40760
IC6		TL431

Reference	Value	Component
J1		CONN353MV2
J2		BNC
J3		BNC
J4		BNC
J5		CONN1X3V_FCON
J6		CONN1X3V_FCON
J7		BNC
J8		BNC
J9		CONN1X3V_FCON
J10		CONN1X3V_FCON
K1		3 POINT JUMPER
K2		3 POINT JUMPER
K3		SWITCH
K4		SWITCH
K5		3 POINT JUMPER
L1	12µH	LQH4N
L2	12µH	LQH4N
L3	12µH	LQH4N
L4	12µH	LQH4N
L5	12µH	LQH4N
L6	12µH	LQH4N
L7	12µH	LQH4N
P1	1K	3224W
P2	1K	3224W
P3	1K	3224W
P4	5K	3224W
Q1	20MHz	X071009
R1	1K	RMR01
R2	470	RMR01
R3	50	RMR01
R4	50	RMR01
R5	80	RMR01
R6	50	RMR01
R7	1K	RMR01
R8	50	RMR01

Reference	Value	Component
R9	470	RMR01
R10	38	RMR01
R11	1K	RMR01
R12	470	RMR01
TC1-TC10		SOLDER POINTS
TP1-TP2	J13	TEST POINTS (jumper)
TP3-TP6		TEST POINTS 2 BIT CONNECTOR (MSBs)
TP7-TP8	J14	TEST POINTS (clock)
TP9-TP10	J15	TEST POINTS (jumper)

11.3 COMPONENT PLACE

(see next page)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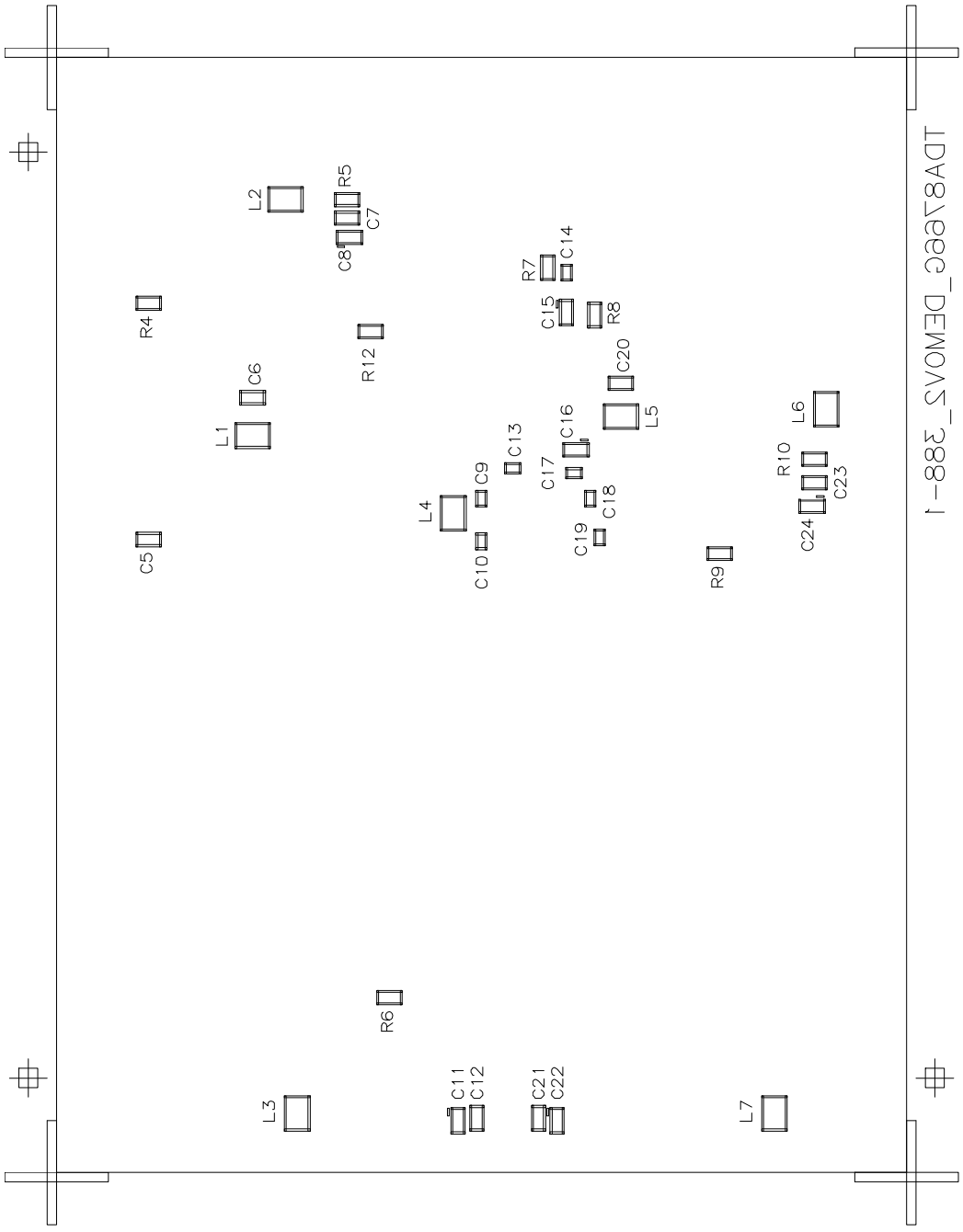
C2
C3
C4
J8
IC5
K5
TP4
TC1
TP6
TC2
TP3
TP5
TC3
TC4
TC5
TC6
TC7
TC8
TC9
TC10
CB2
J1
D1
IC1
J10
J3
IC4
IC6
P2
Q1
TP7
TP8
R11
C1
K4
IC2
K1
R1
K2
K3
R2
D2
J6
J9
TP1
TP2
P1
IC3
TP9
TP10
J7
J5
R3
P4
J2
P3
TDA8766G_DEMOV2_388-1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L2
R5
C7
C8
R7
C14
C15
R8
R4
R12
C20
C6
L1
C16
L5
L6
C13
C17
R10
C9
C18
C23
L4
C19
C24
C5
C10
R9
R6
C11
C12
C21
C22
L3
L7